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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/903,306	07/11/2001	Guangming Lu	MORPHO1180	1006

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EXAMINER	
WILLIAMS, LAWRENCE B	

ART UNIT	PAPER NUMBER
2638	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,306	LU, GUANGMING	
	Examiner	Art Unit	
	Lawrence B. Williams	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Remarks, filed 31 March 2005, with respect to the rejection(s)of claim(s) 1-5, 9-12, 14-17, 20 under 35 USC 102 and claims 6-8, 13, 18, 19 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of DeHon et al. (US Patent 5,742,180).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders (US Patent 6,175,940 B1) in view of DeHon et al. (US Patent 5,742,180).

(1) With regard to claim 1, Saunders discloses in Fig(s). 2-6, discloses a digital signal processing method, comprising: configuring a portion of an array of processing elements for performing a turbo coding routine (col. 2, lines 31-35), and executing the turbo coding routine on data blocks received at the portion of the array of independently processing elements (col. 3, lines 32-39., col. 4, lines 36-46). However, Saunders et al. does not disclose processing element

being independently reconfigurable.

However, DeHon et al. discloses an array of independently reconfigurable processing elements (abstract).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of DeHon et al. with the invention of Saunders as a method of increasing the functionality of the array without increasing hardware.

(2) With regard to claim 2, claim 2 inherits all limitations of claim 1 above. Furthermore, Saunders also discloses in Fig. 5, wherein configuring a portion of the array of processing elements includes activating the portion with an activation signal (signal from programmer controller (30)).

(3) With regard to claim 3, claim 3 inherits all limitations of claim 1 above. Furthermore, Saunders discloses in Fig. 5, wherein the portion of the array of processing elements includes at least one processing element (62).

(4) With regard to claim 4, claim 4 inherits all limitations of claim 1 above. Furthermore, Saunders discloses in Fig. 5, wherein executing the turbo coding routine on data blocks received at a portion of the array of processing elements includes encoding (42, 62) the data blocks.

(5) With regard to claim 5, claim 5 inherits all limitations of claim 1 above. Furthermore, Saunders discloses wherein executing the turbo coding routine on data blocks received at the portion of the array of processing elements includes decoding the data blocks (col. 2, lines 35-38).

(6) With regard to claim 9, claim 9 inherits all limitations of claim 1 above. Furthermore,

Saunders discloses wherein each processing element includes at least one functional unit, and wherein a portion of an array of processing elements for performing a turbo coding routine includes programming the functional unit to perform at least one function of the turbo coding routine (col. 3, lines 32-50).

(7) With regard to claim 10, claim 10 inherits all limitations of claim 9 above. Furthermore, Saunders also discloses wherein the function unit includes programmable logic that is configurable for performing a logical function (col. 3, lines 43-50).

4. Claim 6, 7, 13, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders (US Patent 6,175,940 B1) in combination with of DeHon et al. (US Patent 5,742,180) and further in view of Nguyen (US Patent 6,813,742 B1).

(1) With regard to claim 6, claim 6 inherits all limitations of claim 1 above. As noted above, Saunders in combination with DeHon et al. disclose all limitations of claim 1 above. They do not however disclose wherein configuring a portion of an array of independently reconfigurable processing elements for performing a turbo coding routine includes configuring the portion as a logarithmic maximum a posteriori (LOG-MAP) –based processor.

However, Nguyen discloses wherein a logarithmic maximum a posteriori (LOG-MAP) – based processor (claim 3).

It would have been obvious to one skilled in the art at the time of invention to use the method Nguyen with the invention of Saunders in combination with DeHon et al. as a well known and proven method of implementing iterative decoding of turbo codes.

(2) With regard to claim 7, both DeHon et al. (col. 6, line 66 - col. 7, line 6) and Nguyen (col. 8, line 61 –col. 9, line 4) also discloses method of claim 6 further comprising configuring the portion to access a look-up table.

(3) With regard to claim 13, Nguyen discloses his processor subsystem implemented in an ASIC (application specific integrated circuit) of a SoC (system-on-chip) device, or in a VLSI device for wireless communication applications.

(4) With regard to claim 19, claim 19 inherits all limitations of claims 11 and 6 above.

5. Claim 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders (US Patent 6,175,940 B1) in combination with of DeHon et al. (US Patent 5,742,180) as applied to claims 1 and 11 above and further in view of Stephen et al. (US Patent 6,484,283 B2).

(1) With regard to claim 8, as noted above, Saunders in combination with of DeHon et al. disclose all limitations of claim 1 above. They do not however disclose idling all processing elements in the array other than the portion of processing elements configured for performing the turbo coding routine.

However, Stephen et al. discloses an idling state in his invention of encoding and decoding turbo codes as a measure of power consumption (col. 31, lines 4-23).

It would have been obvious to one skilled in the art at the time of invention to apply the method of Stephen et al. to the invention of Saunders and DeHon et al as a measure to lower power consumption.

(2) With regard to claim 18, claim 18 inherits all limitations of claims 11 and 8 above.

6. Claims 11-17, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeHon et al. (US Patent 5,742,180) in view of Saunders (US Patent 6,175,940 B1)

(1) With regard to claim 11, DeHon et al. discloses in Fig. 1, a digital signal processing apparatus, comprising: an array (100) of interconnected processing elements, each processing element being independently programmable with a context instruction (claim 1); a context memory connected to the array for storing and providing the context instruction to the processing elements (col. 6, lines 54-65); and a processor (118) connected to the array and to the context memory, for controlling the loading of the context instruction to the processing elements.

DeHon et al. does not however teach the processor for configuring a portion the processing elements to perform a turbo coding routine

However Saunders teaches a processor configuring a portion of the processing elements to perform a turbo coding routine (col. 3, lines 43-50).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Saunders with the invention DeHon et al. as a technique to exploit improved coding and decoding techniques for high speed data transmissions (col. 1, lines 33-46).

(9) With regard to claim 12, Saunders also discloses wherein the processor is further configured to execute the turbo coding routine by controlling a state of the configured portion of processing elements (col. 3, lines 42-50).

(9) With regard to claim 14, claim 14 inherits all limitations of claim 11 above. Furthermore, Saunders also discloses in Fig. 5, wherein the turbo coding routine is an encoding process on data blocks received at the portion of the array (col. 2, lines 31-35).

(10) With regard to claim 15, claim 15 inherits all limitations of claim 11 above.

Furthermore, Saunders also discloses in Fig. 6, wherein the turbo coding routine is a decoding process on data blocks received at the portion of the array (col. 2, lines 35-28).

(11) With regard to claim 16, DeHon et al. also discloses wherein each processing element includes at least one functional unit that is programmable for various mathematical functionalities. It would be inherent that the functional units could be programmed to perform at least one function of a turbo coding routine.

(12) With regard to claim 17, DeHon et al also discloses wherein the functional unit includes programmable logic that is configurable by the context instruction (abstract).

(13) With regard to claim 20, claim 20 inherits all limitations of claim 11 above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.) Durbeck et al. discloses in US Patent 6,222,381 B1 Self-Configurable Parallel Processing System Made From Self-Dual Code/Data Processing Cells Utilizing A Non-Shifting Memory.

b.) Vorbach et al. discloses in US Patent 6,119,181 I/O And Memory Bus system For Deps And Units With Two-Or Multi-Dimensional Programmable Cell Architecture.

c.) Vorbach et al. discloses in US Patent 6,088,795 Process For Automatic Dynamic Reloading Of Data Flow Processors (DEPS) And Units With Two Or Three Dimensional Programmable Cell Architectures (FPGAS, DPGAS And The Like).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
June 12, 2005

CHIEH M. FAN
PRIMARY EXAMINER